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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
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ART UNIT	PAPER NUMBER
1791	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/524,778	UMENO ET AL.	
	Examiner	Art Unit	
	SEYED M. MALEKZADEH	1791	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-22,24-26,28-30,32-34,36-38 and 40-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-22,24-26,28-30,32-34,36-38 and 40-45* is/are rejected.

7)☒ Claim(s) *34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/14/2008 has been entered.

Response to Amendment

Claims 20-22, 24-26, 28-30, 28-30, 32-34, 36-38, and 40-45 are pending.

Claims 1-19, 23, 27, 31, 35, 39, and 46-47 are cancelled.

In view of the amendment, filed on 07/14/2008, following rejections are withdrawn from the previous office action, mailed on 01/14/2008 for the reason of record.

- Rejection of claims 20 and 24 over Fusegawa et al. (US 2003/0106484) in view of JP (2003-297840)
- Rejection of claims 21 and 25 over Fusegawa et al ('484) in view of JP (2003-297840) and further in view of Haas et al (US 4,119,441)

- Rejection of claims 22 and 26 over Fusegawa et al ('484) in view of JP (2003-297840) and further in view of Asayama et al (US 6,641,888)
- Rejection of claims 28, 32, 36, 40, and 41 over Fusegawa et al ('484), in view of JP (2003-297840), and further in view of Momoi et al (US 2002/0024152)
- Rejection of claim 29 over Fusegawa et al ('484), JP (2003-297840) in view of Haas et al (US 4,119,441) and further in view of Momoi et al. (US 2002/0024152)
- Rejection of claim 30 over Fusegawa et al ('484), JP (2003-297840) in view of Asayama et al. (US 6,641,888), and further in view of Momoi et al. (US 2002/0024152)
- Rejection of claims 33, 37, and 42-43 over Fusegawa et al ('484), JP (2003-297840) in view of Momoi et al. ('152), and further in view of Haas et al (US '441)
- Rejection of claims 34, 38, 44-45 over Fusegawa et al ('484), JP ('840) in view of Momoi et al ('152) and further in view of Asayayama et al (6,641,888)

New Ground of Rejections

Claim Objections

Claim 34 is objected to because of the following informalities: in claim 1, lines 4-5, the recitation “nitrogen by a concentration of $2\times10^{13}\,atoms/cm^3$ of more” requires modification. The citation “of more” should be modified to "or more”. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 20-22, 24-26, 28-30, 40-45 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 20 recites the limitation "the silicon wafer not including COP" in eight and ninth lines of the claim. There is insufficient antecedent basis for this limitation in the claim because prior to the cited limitation, the claim fails to clearly define “a silicon wafer not including COP”

Claims 28-30 provide a manufacturing method of a SOI wafer by the use of a silicon wafer not including COP in which the silicon wafer is manufactured by another manufacturing method, but, since the claim does not set forth any steps involved in the method, it is unclear what method/process applicant is intending to encompass. A claim is indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

The phrase "predetermined temperature" in the claim 40, line 28 renders the claim indefinite. The term "predetermined" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the claim.

Claim 41 recite the limitation "the separated active layer side wafer" in the second and third lines of the claim. There is insufficient antecedent basis for this limitation in the claim because prior to the cited limitation, the preceded recitations fail to clearly define “a separated active layer side wafer”

Claim 41 recites the limitation "it can be used" in the third line of the claim. There is insufficient antecedent basis for this limitation in the claim because it is not clear in which the recitation “it” refers to which of the preceded process steps or products by the process.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 20, 22, 24, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hölzl et al. (US 6,803,331) in view of Hull, R. "Properties of Crystalline Silicon", The institution of Electrical Engineers, London, 1999, the prior art submitted by the applicants.

Hölzl et al. (US '331) teach a manufacturing process of a silicon single crystal wafer which is free of COPs, wherein the process includes the step of preparing a silicon single crystal by growing a silicon single crystal through the Czochralski method, and dividing the silicon single crystal into the wafers as a slicing step to slice a silicon wafer containing COPs from the obtained silicon single crystal. Moreover, Hölzl et al. (US '331) teach the step of heat treating the silicon wafer which contains COPs in an oxygen-containing atmosphere to obtain a silicon wafer free of COPs not only in a layer close to the surface of the silicon wafer, but also over a significant part of the wafer thickness (See lines 40-45, column 10; lines 51-58, column 4; and lines 25-29, column 5) in such a

way that the heat treatment takes place at a temperature which is selected in such a way to satisfy the following inequality:

$$[O_i] < [O_i]^{eq}(T)\exp(\frac{2\sigma_{SiO2}\Omega}{rkT})$$

Wherein $[O_i]$ is the concentration of the interstitial oxygen, $[O_i]^{eq}(T)$ is the limit solubility of oxygen in silicon at a temperature T, σ_{SiO2} is the surface energy of silicon oxide, Ω is the volume of a precipitated oxygen atom, r is the mean COP radius, and k is the Boltzman constant. (See abstract)

Furthermore, the prior art teach through subjecting the silicon single crystal wafer to a heat treatment process, the COPs within the silicon wafer vanishes, and then the wafer is subjected to a final or mirror polishing step in which results in a perfect silicon wafer surface condition. (See lines 13-25, column 10)

Hölzl et al. (US '331) also teach it is preferable to add nitrogen, as a doping element, to the silicon melt during the pulling process of the silicon single crystal to further reduce the mean COP size within the silicon single crystal in such a way that the nitrogen concentration in the silicon single crystal or in the produced silicon wafer is in the range between $1\times10^{13} atoms/cm^3$ and $7\times10^{15} atoms/cm^3$. (See lines 12-18, column 6)

However, the prior art is silent about values of $[O_i]^{eq}(T)$ and $\frac{2\sigma_{SiO2}\Omega}{r}$, as annealing parameters, in which each has a constant value in such a way that

$[O_i]$ varies with the variation of (T) in the silicon wafer heat treatment process, as claimed in claim 20.

In the analogous art, Hull, R. teaches a method for producing a silicon single crystal through Czochralski process in which the produced silicon single crystal wafer is subjected to an annealing step after manufacturing step in such a way that the interstitial oxygen concentration of the silicon single crystal varies with the variation of the annealing temperature.

Furthermore, the prior art teach through analyzing experimental results obtained from the silicon annealing process and then bringing together the experimental data and combining the data with the different annealing factors, the silicon heat treatment temperature and the interstitial oxygen concentration yield on a curve which satisfies the following equation:

$$[O_{eq}]_{sol} = 9.0\times10^{22}\exp(-1.76\times10^{4}(K)/T)cm^{-3}$$

Also, the prior art teach precise adjustment of the annealing parameters allows production of CZ silicon crystals with fairly uniform and controlled distribution of dislocations within the surface of the silicon single crystal. (See Hull, R. “Properties of Crystalline Silicon", The institution of Electrical Engineers, London, 1999, PP 489-450, section C)

Therefore, it would have been obvious for one of ordinary skill in the art at the time of applicant’s invention to modify the manufacturing method of a silicon single crystal wafer as taught by Hölzl et al. (US ‘331) through providing constant values for the annealing parameters in such a way that the

concentration of interstitial oxygen varies with the variation of the annealing temperature in order to minimize distribution of the dislocations and crystalline defects throughout the silicon single crystal wafer surface, as suggested by Hull, R.

Claims 21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hölzl et al. (US 6,803,331) in view of Hull, R. as applied to claims 20, 22, 24, and 26, and further in view of Haas et al (US 4,119,441)

The combined teachings of Hölzl et al. (US 6,803,331) and Hull, R. disclose all the process limitations of manufacturing method of a silicon single crystal wafer but do not teach that the sliced silicon single crystal is doped with phosphorus through a neutron irradiation process.

In the analogous art, Haas et al ('441) teach a method for the production of n-doped silicon single crystal which has a region of elevated specific electric resistance at its center wherein the silicon single crystal is exposed to a neutron irradiation in order to dope the silicon single crystal with phosphorus. The prior art further teaches the neutron radiation causes a weaker doping concentration in marginal regions of the crystals due to the production of fewer phosphorous atoms. (See abstract)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify the silicon wafer manufacturing process taught by combined teachings of Hölzl et al. (US 6,803,331) and Hull,

R, through providing a phosphorous doping step of the silicon wafer in order to decrease crystal damage and making a specific resistance in the silicon single crystal wafer, as suggested by Hass et al. ('441)

Claims 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hölzl et al. (US 6,803,331) in view of Hull, R., as applied to claims 20, 22, 24, and 26 above, and further in view of Momoi et al (US 2002/0024152)

The combined teachings of Hölzl et al. (US 6,803,331) and Hull, R. disclose all the process limitations of a manufacturing method of silicon single crystal wafer; however, the prior arts fail to teach a SOI wafer fabricating step by using the COP-free silicon wafer obtained by silicon single crystal manufacturing process claimed in claims 20, 22, 24, and 26.

In the analogous art, Momoi et al (US '152) disclose a method of manufacturing SOI wafer comprising a silicon substrate, an insulating layer formed in the substrate, and a semiconductor layer formed over the insulating layer in which the silicon substrate is a silicon single crystal wafer fabricated by the Czochralski process (See paragraph [0002], [0005], [0113], and claim 37), wherein SOI wafer (1) includes substrate (2), buried insulating layer (3) formed on the substrate (2), and single-crystal semiconductor layer (4) formed on the buried insulating layer (3). (See paragraph [0113])

Therefore, it would have been obvious for one of ordinary skill in the art at the time of applicant's invention to modify the silicon wafer manufacturing

process taught by combined teachings of Hölzl et al. (US 6,803,331) and Hull, R. through providing a SOI wafer fabricating step by using the COP-free silicon wafer in order to reduce a signal transmission loss of a semiconductor device by providing SOI substrate in the semiconductor system, as suggested by Momoi et al (US '152).

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hölzl et al. (US 6,803,331) in view of Hull, R, and further in view of Haas et al (US 4,119,441), as applied to claims 21 and 25 above, and further in view of Momoi et al (US 2002/0024152)

The combined teachings of Hölzl et al. (US 6,803,331) in view of Hull, R. and further in view of Haas et al (US 4,119,441) disclose all the process limitations of a manufacturing method of silicon single crystal wafer; however, the prior arts fail to teach a SOI wafer fabricating step by using the COP-free silicon wafer obtained by silicon single crystal manufacturing process claimed in claims 25 and 26.

In the analogous art, Momoi et al (US '152) disclose a method of manufacturing SOI wafer comprising a silicon substrate, an insulating layer formed in the substrate, and a semiconductor layer formed over the insulating layer in which the silicon substrate is a silicon single crystal wafer fabricated by the Czochralski process (See paragraph [0002], [0005], [0113], and claim 37), wherein SOI wafer (1) includes substrate (2), buried insulating layer (3)

formed on the substrate (2), and single-crystal semiconductor layer (4) formed on the buried insulating layer (3). (See paragraph [0113])

Therefore, it would have been obvious for one of ordinary skill in the art at the time of applicant's invention to modify the silicon wafer manufacturing process taught by combined teachings of Hölzl et al. (US 6,803,331), Hull, R, and Haas et al (US 4,119,441) through providing a SOI wafer fabricating step by using the COP-free silicon wafer in order to reduce a signal transmission loss of a semiconductor device by providing SOI substrate in the semiconductor system, as suggested by Momoi et al (US '152)

Claims 32, 34, 36, 38, 40, 41, and 43-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Momoi et al. (US 2002/0024152) in view of Hull, R. and Hölzl et al. (US 6,803,331)

Momoi et al (US 2002/0024152) disclose a method of manufacturing SOI wafer comprising a silicon substrate, an insulating layer formed in the substrate, and a semiconductor layer formed over the insulating layer in which the silicon substrate is a silicon single crystal wafer fabricated by the Czochralski process (See paragraph [0002], [0005], [0113], and claim 37), wherein SOI wafer (1) includes substrate (2), buried insulating layer (3) formed on the substrate (2), and single-crystal semiconductor layer (4) formed on the buried insulating layer (3). (See paragraph [0113])

Furthermore, Momoi et al (US '152) teach the active region (103') as an active layer side silicon wafer is formed on a buried insulating layer (104) of the

SOI wafer which is patterned in the form of islands. (See paragraph [0189]) Moreover, Momoi et al (US '152) teach an insulating layer (14) composed of silicon oxide is formed on the substrate (11) with a semiconductor layer (13) by a technique such as thermal oxidation. (See paragraph [0176])

Therefore, Momoi et al (US '152) teach a buried oxide film is formed on the SOI wafer by applying a heat treatment to an active layer side silicon wafer (See paragraph [0081] and [0093])

Furthermore, Momoi et al (US '152) teach the silicon wafer is then bonded to a supporting side wafer with a buried oxide layer interposed there-between (See paragraphs [0151] and [0189]). Also, Momoi et al (US '152) teach a heat treatment for improving a bonding strength is performed at a temperature equal to or higher than 900° C. (See paragraph [0054])

Therefore, Momoi et al (US '152) teach a manufacturing method of a SOI wafer, in which a buried oxide film is formed by applying a heat treatment to an active layer side silicon wafer in an oxidizing atmosphere and the active layer side silicon wafer is then bonded to a supporting side wafer with the buried oxide layer interposed there between to manufacture a bonded SOI wafer.

Moreover, Momoi et al (US '152) teach the manufacturing method of SOI wafers have two steps which are a separation step by ion-implanted oxygen (SIMOX) process in which the oxygen ions are implanted into the silicon single-crystal substrate to form an insulating layer, and a bonding process in which

two different semiconductor substrates are bonded and a single-crystal semiconductor layer is formed by polishing or separation. (See paragraph [0019]) Furthermore, the prior art teach the separation layer is an oxide film layer formed by ion implantation. (See paragraphs [0020] and [0062])

Therefore, Momoi et al (US '152) teach forming an ion implanted layer in the active layer side silicon wafer not including COP by forming an oxide film on the active layer side silicon wafer by ion implanting process, and also forming a bonded wafer by bonding the active layer side silicon wafer having the ion implanted layer to a supporting side wafer with the oxide film interposed there between; furthermore, separating a part of the active layer side silicon wafer from a boundary defined by the ion implanted layer by holding the bonded wafer at a predetermined temperature to apply a heat treatment thereto.

Moreover, Momoi et al (US '152) teach a porous layer (12) as an active layer side silicon wafer is formed on the surface of first substrate (11) wherein the porous layer (12) is a porous single-crystal silicon, and the first substrate (11) is made of a semiconductor material such as silicon in which the porous layer (12) is subjected to a heat treatment at about 400°C in an oxidizing atmosphere to form a film of silicon oxide on the inner walls of the porous layer (12) as the active layer side silicon wafer. (See paragraph [0157])

However, Momoi et al (US '152) does not teach that the active layer side silicon wafer includes interstitial oxygen with a concentration $[O_i]$ in which the

interstitial oxygen concentration varies with the heat treatment temperature(T); furthermore, the prior art fails to teach the COPs throughout the active layer side silicon wafer vanishes after the heat treatment step of the silicon wafer and also the surface of the active layer is mirror polished; moreover, the prior art fail to teach the silicon single crystal used for the fabrication of SOI wafer is doped with nitrogen by a concentration of $2 \times 10^{13} atoms/cm^3$ or more or doped with carbon by a concentration of $5 \times 10^{16} atoms/cm^3$ or more.

In the analogous art, Hull, R. teaches a method for producing a silicon single crystal through Czochralski process in which the produced silicon single crystal wafer is subjected to an annealing step after manufacturing step in such a way that the interstitial oxygen concentration of the silicon single crystal varies with the variation of the annealing temperature.

Furthermore, the prior art teach through analyzing experimental results obtained from the silicon annealing process and then bringing together the experimental data and combining the data with the different annealing factors, the silicon heat treatment temperature and the interstitial oxygen concentration yield on a curve which satisfies the following equation:

$$[O_{eq}]_{sol} = 9.0 \times 10^{22} \exp(-1.76 \times 10^4 (K)/T) cm^{-3}$$

Also, the prior art teach precise adjustment of the annealing parameters allows production of CZ silicon crystals with fairly uniform and controlled

distribution of dislocations within the surface of the silicon single crystal. (See Hull, R. "Properties of Crystalline Silicon", The institution of Electrical Engineers, London, 1999, PP 489-450, section C)

In another analogous art, Hölzl et al. (US '331) teach a manufacturing process of a silicon single crystal wafer which is free of COPs, wherein the process includes the step of preparing a silicon single crystal by growing a silicon single crystal through the Czochralski method, and dividing the silicon single crystal into the wafers as a slicing step to slice a silicon wafer containing COPs from the obtained silicon single crystal. Moreover, Hölzl et al. (US '331) teach the step of heat treating the silicon wafer which contains COPs in an oxygen-containing atmosphere to obtain a silicon wafer free of COPs not only in a layer close to the surface of the silicon wafer, but also over a significant part of the wafer thickness.(See lines 40-45, column 10; lines 51-58, column 4; and lines 25-29, column 5) in such a way that the heat treatment takes place at a temperature which is selected in such a way to satisfy the following inequality:

$$[O_i] < [O_i]^{eq}(T)\exp(\frac{2\sigma_{SiO2}\Omega}{rkT})$$

Wherein $[O_i]$ is the concentration of the interstitial oxygen, $[O_i]^{eq}(T)$ is the limit solubility of oxygen in silicon at a temperature T, σ_{SiO2} is the surface energy of silicon oxide, Ω is the volume of a precipitated oxygen atom, r is the mean COP radius, and k is the Boltzman constant. (See abstract)

Furthermore, the prior art teach through subjecting the silicon single crystal wafer to a heat treatment process, the COPs within the silicon wafer vanishes, and then the wafer is subjected to a final or mirror polishing step in which result in a perfect silicon wafer surface condition. (See lines 13-25, column 10)

Hölzl et al. (US '331) also teach it is preferable to add nitrogen, as a doping element, to the silicon melt during the pulling process of the silicon single crystal to further reduce the mean COP size within the silicon single crystal in such a way that the nitrogen concentration in the silicon single crystal or in the produced silicon wafer is in the range between $1\times10^{13}\,atoms/cm^3$ and $7\times10^{15}\,atoms/cm^3$.

Therefore, it would have been obvious for one of ordinary skill in the art at the time of applicant's invention to modify the manufacturing method of a SOI wafer as taught by Momoi et al (US '152) through providing a relationship between the concentration of interstitial oxygen $[O_i]$ with the annealing temperature (T) of the active layer side silicon wafer in order to minimize the dislocations and crystalline defects throughout the silicon single crystal wafer surface, as suggested by Hull, R.

Also, it would have been obvious for one of ordinary skill in the art at the time of applicant's invention to modify the manufacturing method of a SOI wafer as taught by Momoi et al (US '152) through providing a step of removing the COPs throughout the active layer side silicon wafer when subjecting the

wafer to a heat treatment process and mirror polishing the surface of the active layer in order to improve the quality of the silicon wafer through minimizing the number of defects within the silicon single crystal layer, and further providing a doping step to dope the silicon single crystal with nitrogen by a concentration of $2\times10^{13}\,atoms/cm^3$ or more in order to reduce the mean COP size within the silicon single crystal during the pulling process of the silicon single crystal by CZ method, as suggested by Hölzl et al (US '331)

Claims 33, 37, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Momoi et al (US '152) in view of Hull, R. and Hölzl et al (US 331), as applied to claims 32, 34, 36, 38, 40, 41, and 43-45 and further in view of Haas et al (US 4,119,441)

The combined teachings of Momoi et al (US '152) in view of Hull, R. and Hölzl et al (US 331) disclose all the process limitations of manufacturing method of a SOI wafer but do not teach that the active layer side silicon wafer is doped with phosphorus through a neutron irradiation process.

In the analogous art, Haas et al ('441) teach a method for the production of n-doped silicon single crystal which has a region of elevated specific electric resistance at its center wherein the silicon single crystal is exposed to a neutron irradiation in order to dope the silicon single crystal with phosphorus. The prior art further teaches the neutron radiation causes a weaker doping concentration in marginal regions of the crystals due to the production of fewer phosphorous atoms. (See abstract)

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify the silicon wafer manufacturing process taught by combined teachings of Hölzl et al. (US 6,803,331) and Hull, R. (Ed.) through providing a phosphorous doping step of the silicon wafer in order to decrease crystal damage and making a specific resistance in the silicon single crystal wafer, as suggested by Hass et al. ('441)

Response to Arguments

Applicant's arguments with respect to claims 20-22, 24-26, 28-30, 32-34, 36-38, and 40-45 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seyed Masoud Malekzadeh whose telephone number is 571-272-6215. The examiner can normally be reached on Monday – Friday at 8:30 am – 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven P. Griffin, can be reached on (571) 272-1189. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published application may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance form a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. M. M./

Examiner, Art Unit 1791

/Steven P. Griffin/

Supervisory Patent Examiner, Art Unit 1791